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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
AHLUWALIA, NAVNEET K	
ART UNIT	**PAPER NUMBER**
2166	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/767,776	BIRDWELL ET AL.	
	Examiner	Art Unit	
	Navneet K. Ahluwalia	2166	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *42,44-66 and 68-76* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *42,44-66,68-76* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 04/20/2007 has been entered.

Response to Arguments

2. Claims 42, 44 – 66, 68 – 76 are pending in this Office Action. After a thorough examination of the present application, claims 42, 44 – 66, 68 – 76 remain rejected. Applicant's arguments filed with respect to claims 42, 44 – 66, 68 – 76 have been fully considered but they are not persuasive.

***First**, Applicant argues that there is no teaching in Merkey communicating both capacity and load.*

In response to Applicant's argument, the Examiner submits that Merky teaches the communication of both the load and capacity of processors in column 9 lines 31 – 40, Merkey. It discloses a load indicator, which indicated how heavily the corresponding processor is loaded. Furthermore, the load indicator provides a measure indicating how

much of available processing capacity is being spent running code in application threads versus an idle thread.

***Second**, Applicant argues that there is no teaching in Merkey of a communication system...wherein at least two host processors communicate capacity and load to other processors.*

In response to Applicant's argument, the Examiner submits that Merky teaches the communication of the capacity and load to other processors in column 9 lines 31 – 58, Merkey. It discloses the communication of the load and capacity between processors. Furthermore, support for this communication is also disclosed in column 10 lines 59 – 67, Merkey.

Other claims recite the same subject matter and for the same reasons as cited above the rejection is maintained.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 42, 44 – 66, 68 – 76 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeffrey V. Merkey ('Merkey' herein after) (US 6,728,959 B1) further in view of Kitain et al. ('Kitain' herein after) (US 5,864,871).

With respect to claim 42,

Merkey discloses a parallel data processing architecture for search, storage and retrieval of data, said parallel data processing architecture comprising: a plurality of host processors including a root host processor (Figure 2 and 5, Merkey), said root host processor being responsive to client queries (Figure 5 element 60, Merkey) wherein at least two host processors have a search engine and maintain information of a search queue (Figure 6,l Merkey and column 6 lines 24 – 27, Kitain); each of said host and root host processors maintaining a list of available host processors and information about the capacity and load for each available host processor in memory (Figures 7 and 8, Merkey) and broadcasting its capacity and load information to other host processors and bringing its search queue into balance with another host processor in response to receipt of said broadcast capacity and load information according to a time constant (Figure 7 and column 9 lines 30 – 40, Merkey); and a communication system coupling

said host and root host processors, selected host processors storing a database index in memory comprising nodes and data accessible via said nodes (Figure 9, Merkey).

Merkey however does not disclose the search, storage and retrieval of data and the database index as claimed.

Kitain teaches the search, storage and retrieval of data and the database index as claimed (column 6 lines 12 – 27 and column 16 lines 44 – 47, Kitain).

6. It would have been obvious to one of ordinary skill in the art of data processing at the time of the present invention to combine the teachings of cited references because the communication between the processors would ensure an efficient search engine being used to obtain the search results and allows more than one search to be conducted in parallel (column 6 lines 21 – 27, Kitain). Furthermore, with the global dispatch queue the load balancing of the processors would make the processing much more efficient (column 16 lines 44 – 47, Kitain).

With respect to claim 44,

Merkey discloses a parallel data processing architecture for search, storage and retrieval of data, said parallel data processing architecture comprising: a plurality of host processors including a root host processor (Figure 2 and 5, Merkey), said root host processor being responsive to client queries (Figure 5 element 60, Merkey) wherein at least two host processors have a search engine and maintain information of a search queue; each of said host and root host processors maintaining a list of available host processors and information about the capacity and load for each available host

processor in memory (Figures 7 and 8, Merkey) and broadcasting its capacity and load information to other host processors and bringing its search queue into balance with another host processor in response to receipt of said broadcast capacity and load information according to a time constant; and a communication system coupling said host and root host processors, selected host processors storing a database index in memory comprising nodes and data accessible via said nodes (Figure 9, Merkey) wherein the plurality of host processors comprises three host processors, of which two host processors have search engines (column 6 lines 24 – 27, Kitain) and maintain information of a search queue and the third comprises said root host processor (Figure 6, Merkey).

Merkey however does not disclose the search, storage and retrieval of data and the database index as claimed.

Kitain teaches the search, storage and retrieval of data and the database index as claimed (column 6 lines 12 – 27 and column 16 lines 44 – 47, Kitain).

It would have been obvious to one of ordinary skill in the art of data processing at the time of the present invention to combine the teachings of cited references because the communication between the processors would ensure an efficient search engine being used to obtain the search results and allows more than one search to be conducted in parallel (column 6 lines 21 – 27, Kitain). Furthermore, with the global dispatch queue the load balancing of the processors would make the processing much more efficient (column 16 lines 44 – 47, Kitain).

With respect to claim 45,

Merkey discloses a parallel data processing architecture for search, storage and retrieval of data, said parallel data processing architecture comprising: a plurality of host processors including a root host processor (Figure 2 and 5, Merkey), said root host processor being responsive to client queries (Figure 5 element 60, Merkey) wherein at least two host processors have a search engine and maintain information of a search queue; each of said host and root host processors maintaining a list of available host processors and information about the capacity and load for each available host processor in memory (Figures 7 and 8, Merkey) and broadcasting its capacity and load information to other host processors and bringing its search queue into balance with another host processor in response to receipt of said broadcast capacity and load information according to a time constant; and a communication system coupling said host and root host processors, selected host processors storing a database index in memory comprising nodes and data accessible via said nodes (Figure 9, Merkey) wherein the plurality of host processors comprises two host processors, of which one comprises said root host and both said host processors have search engines (column 6 lines 24 – 27, Kitain) and maintain information of a search queue (Figure 6, Merkey).

Merkey however does not disclose the search, storage and retrieval of data and the database index as claimed.

Kitain teaches the search, storage and retrieval of data and the database index as claimed (column 6 lines 12 – 27 and column 16 lines 44 – 47, Kitain).

It would have been obvious to one of ordinary skill in the art of data processing at the time of the present invention to combine the teachings of cited references because the communication between the processors would ensure an efficient search engine being used to obtain the search results and allows more than one search to be conducted in parallel (column 6 lines 21 – 27, Kitain). Furthermore, with the global dispatch queue the load balancing of the processors would make the processing much more efficient (column 16 lines 44 – 47, Kitain).

With respect to claim 46,

Merkey discloses a parallel data processing architecture for search, storage and retrieval of data, said parallel data processing architecture comprising: a plurality of host processors including a root host processor (Figure 2 and 5, Merkey), said root host processor being responsive to client queries (Figure 5 element 60, Merkey) wherein at least two host processors have a search engine and maintain information of a search queue; each of said host and root host processors maintaining a list of available host processors and information about the capacity and load for each available host processor in memory (Figures 7 and 8, Merkey) and broadcasting its capacity and load information to other host processors and bringing its search queue into balance with another host processor in response to receipt of said broadcast capacity and load information according to a time constant; and a communication system coupling said host and root host processors, selected host processors storing a database index in memory comprising nodes and data accessible via said nodes (Figure 9, Merkey)., the

root host processor being responsive to a client query and using an initial search queue (Figure 4 and column 11 lines 42 – 53, Kitain).

Merkey however does not disclose the search, storage and retrieval of data and the database index as claimed.

Kitain teaches the search, storage and retrieval of data and the database index as claimed (column 6 lines 12 – 27 and column 16 lines 44 – 47, Kitain).

It would have been obvious to one of ordinary skill in the art of data processing at the time of the present invention to combine the teachings of cited references because the communication between the processors would ensure an efficient search engine being used to obtain the search results and allows more than one search to be conducted in parallel (column 6 lines 21 – 27, Kitain). Furthermore, with the global dispatch queue the load balancing of the processors would make the processing much more efficient (column 16 lines 44 – 47, Kitain).

With respect to claim 48,

Merkey discloses a parallel data processing architecture for search, storage and retrieval of data, said parallel data processing architecture comprising: a plurality of host processors including a root host processor (Figure 2 and 5, Merkey), said root host processor being responsive to client queries (Figure 5 element 60, Merkey) wherein at least two host processors have a search engine and maintain information of a search queue; each of said host and root host processors maintaining a list of available host processors and information about the capacity and load for each available host

processor in memory (Figures 7 and 8, Merkey) and broadcasting its capacity and load information to other host processors and bringing its search queue into balance with another host processor in response to receipt of said broadcast capacity and load information according to a time constant; and a communication system coupling said host and root host processors, selected host processors storing a database index in memory comprising nodes and data accessible via said nodes (Figure 9, Merkey)., the root host processor being responsive to a client query and selecting a host processor (Figure 6, Merkey) to receive search request information (column 16 lines 44 – 47, Kitain).

Merkey however does not disclose the search, storage and retrieval of data and the database index as claimed.

Kitain teaches the search, storage and retrieval of data and the database index as claimed (column 6 lines 12 – 27 and column 16 lines 44 – 47, Kitain).

It would have been obvious to one of ordinary skill in the art of data processing at the time of the present invention to combine the teachings of cited references because the communication between the processors would ensure an efficient search engine being used to obtain the search results and allows more than one search to be conducted in parallel (column 6 lines 21 – 27, Kitain). Furthermore, with the global dispatch queue the load balancing of the processors would make the processing much more efficient (column 16 lines 44 – 47, Kitain).

Claims 47, 49 – 65, 75 – 76 are rejected under the same rationale given for claims 42, 44, 45, 47 and 48. The citations of the elements claimed and taught are listed below.

With respect to claim 47,

Kitain teaches the parallel data processing architecture of claim 46, the root host processor creating a search client object (column 8 lines 27 – 49, Kitain).

With respect to claim 49,

Merkey discloses the parallel data processing architecture of claim 42: each host processor reconfiguring information on available host processors in response to the receipt of broadcast information (Figures 6, 7 and column 9 lines 30 – 40, Merkey).

With respect to claim 50,

Merkey discloses the parallel data processing architecture of claim 49 wherein the information on available host processors at each available host processor changes in response to failure of a host processor (column 9 lines 41 – 49, Merkey).

With respect to claim 51,

Merkey discloses the parallel data processing architecture of claim 49 wherein the information on available host processors at each available host processor changes in response to the addition of a host processor (Figure 9, Merkey).

With respect to claim 52,

Merkey discloses the parallel data processing architecture of claim 42 wherein said plurality of host processors comprises groups of host processors (Figure 2, Merkey).

With respect to claim 53,

Kitain teaches the parallel data processing architecture of claim 52, all host processors in each group operating on the same database (Figure 5, Kitain).

With respect to claim 54,

Kitain teaches the parallel data processing architecture of claim 52, each group being assigned a portion of the database (column 6 lines 12 – 21, Kitain).

With respect to claim 55,

Kitain teaches the parallel data processing architecture of claim 54, each group being assigned a different portion of the database (column 6 lines 12 – 21, Kitain).

With respect to claim 56,

Kitain teaches the parallel data processing architecture of claim 55, wherein each processor of a group of processors is assigned the same portion of the database (Figure 5, Kitain).

With respect to claim 57,

Kitain teaches the parallel data processing architecture of claim 46, wherein said client query requests storage or retrieval of information to be performed and wherein work of said storage or retrieval is distributed among a cooperating group of host processors (column 10 lines 26 – 54, Kitain).

With respect to claim 58,

Merkey discloses the parallel data processing architecture of claim 42, each host processor maintaining a search queue and broadcasting its capacity and load information to other host processors and each host processor bringing its search queue into balance with another host processor responsive to receipt of said broadcast capacity and load information according to a time constant (Figures 6, 7 and column 9 lines 30 – 40, Merkey).

With respect to claim 59,

Merkey discloses the parallel data processing architecture of claim 42, at least two host processors having a queue of search requests, each of said host processors executing a search engine (column 6 lines 24 – 27, Kitain), communicating capacity and load information between host processors and said at least two host processors exchanging at least one search request (Figure 9, Merkey).

With respect to claim 60,

Merkey discloses the parallel data processing architecture of claim 59, the search engine removing at least one search request from a search queue and generating an additional search request (Figure 6, Merkey).

With respect to claim 61,

Kitain teaches the parallel data processing architecture of claim 42, said index being a database tree, said host processors capable of executing a set of tests, associating one test to each non-terminal node of said index (column 6 lines 12 – 27 and column 16 lines 44 – 47, Kitain).

With respect to claim 62,

Merkey discloses the parallel data processing architecture of claim 42, said available host processors comprising groups of m processors where m is an integer greater than 1 (Figure 2 and 3, Merkey).

With respect to claim 63,

Merkey discloses the parallel data processing architecture of claim 42, wherein said communications system is proximately located to said root host processor (Figure 6 element 80 and Figure 7, Merkey).

With respect to claim 64,

Merkey discloses the parallel data processing architecture of claim 42, wherein the plurality of host processors comprises at least two host processors having search engines (column 6 lines 24 – 27, Kitain) and maintaining information of a search queue, one of said host processors processing a search request and generating a new search request (Figure 7 and column 9 lines 30 – 40, Merkey).

With respect to claim 65,

Kitain teaches the parallel data processing architecture of claim 64, said new search request being generated in response to matches accounting for one of match stringency, mismatch, equivalence, number of alleles and measurement error specifications (column 10 lines 33 – 45, Kitain).

With respect to claim 75,

Merky discloses the data processing architecture of claim 42, further comprising shared memory (column lines 38 – 67 and column 2 lines 33 – 54, Merkey).

With respect to claim 76,

Merky discloses the data processing architecture of claim 42, further comprising distributed memory among each processor (column lines 38 – 67 and column 2 lines 33 – 54, Merkey).

With respect to claim 66,

Merkey discloses a parallel data processing architecture for search, storage and retrieval of data responsive to queries, said parallel data processing architecture comprising a) a plurality of host processors comprising at least one root host processor responsive to a client query and at least one host processor (Figure 2 and 5, Merkey); b) a communication system coupling said host processors, said host processors capable of communicating with one another (Figure 9, Merkey); and c) host processor memory, a method of balancing workload between said host processors characterized by the steps of: each of said host processors maintaining capacity and load information of said host processors and of a search queue; each host processor broadcasting its capacity and load information to other host processors according to a time constant; and each host processor bringing its search queue into balance with another host processor responsive to receipt of said broadcast capacity and load information (Figure 7 and column 9 lines 30 – 40, Merkey).

Merkey however does not disclose the search, storage and retrieval of data as claimed.

Kitain teaches the search, storage and retrieval of data as claimed (column 6 lines 12 – 27 and column 16 lines 44 – 47, Kitain).

It would have been obvious to one of ordinary skill in the art of data processing at the time of the present invention to combine the teachings of cited references because the communication between the processors would ensure an efficient search engine being used to obtain the search results and allows more than one search to be conducted in parallel (column 6 lines 21 – 27, Kitain). Furthermore, with the global

dispatch queue the load balancing of the processors would make the processing much more efficient (column 16 lines 44 – 47, Kitain).

7. Claims 68 – 71 are rejected under the same rationale given for claim 66. The citations of the elements claimed and taught are listed below.

With respect to claim 68,

Merkey discloses the method of claim 66 wherein the step of bringing a search queue into balance comprises the step of exchanging a block of search requests between host processors (column 9 lines 30 – 49, Merkey).

With respect to claim 69,

Kitain teaches the method of claim 66 further comprising the step of changing the size of blocks of search requests (Figure 3 element 204, Kitain).

With respect to claim 70,

Merkey discloses the method of claim 66, the root host processor using an initial search queue for a query (Figures 5 and 6, column 9 lines 15 – 23, Merkey).

With respect to claim 71,

Merkey discloses the method of claim 66, the root host processor selecting a search queue of another host processor as an initial search queue (Figures 5 and 6, column 9 lines 15 – 40, Merkey).

With respect to claim 72,

Merkey discloses a parallel data processing architecture for search, storage and retrieval of data responsive to queries, said parallel data processing architecture comprising a) a plurality of available host processors comprising at least one root host processor responsive to a client query and at least one host processor (Figure 2 and 5, Merkey); b) a communication system coupling said available host processors, said available host processors capable of communicating with one another (Figure 9, Merkey); and c) host processor memory, a method of storing information of available host processors comprising the steps of: each host processor maintaining information on said plurality of said available host processors and on their capacity and load; each host processor broadcasting its capacity and load information to other host processors according to a time constant; and each host processor reconfiguring information on available host processors responsive to the receipt of broadcast information (Figure 7 and column 9 lines 30 – 40, Merkey).

Merkey however does not disclose the search, storage and retrieval of data as claimed.

Kitain teaches the search, storage and retrieval of data as claimed (column 6 lines 12 – 27 and column 16 lines 44 – 47, Kitain).

It would have been obvious to one of ordinary skill in the art of data processing at the time of the present invention to combine the teachings of cited references because the communication between the processors would ensure an efficient search engine

being used to obtain the search results and allows more than one search to be conducted in parallel (column 6 lines 21 – 27, Kitain). Furthermore, with the global dispatch queue the load balancing of the processors would make the processing much more efficient (column 16 lines 44 – 47, Kitain).

Claims 73 – 74 are rejected under the same rationale given for claim 72. The citations of the elements claimed and taught are listed below.

With respect to claim 73,

Merkey discloses the method of claim 72 wherein the information on available host processors at each available host processor changes in response to failure of a host processor (column 9 lines 41 – 49, Merkey).

With respect to claim 74,

Merkey discloses the method of claim 72 wherein the information on available host processors at each available host processor changes in response to the addition of a host processor (Figure 9, Merkey).

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Navneet K. Ahluwalia whose telephone number is 571-272-5636.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alam T. Hosain can be reached on 571-272-3978. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Navneet

Navneet K. Ahluwalia
Examiner
Art Unit 2166

MOHAMMAD ALI
PRIMARY EXAMINER

Dated: 06/20/2007